WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate including a first semiconductor layer having a first conductivity and a second semiconductor layer having a second conductivity on said first semiconductor layer, said first semiconductor layer partially having a hollow portion in a first surface opposite to said second semiconductor layer, a surface of said second semiconductor layer opposite to said first semiconductor layer having first and second areas, said first area defined by a thin portion of said semiconductor substrate provided by said hollow portion, said second area being outside said first area;

an integrated circuit portion at said second area;

an impurity diffusion layer with said first conductivity piercing said second semiconductor layer from said surface of said second semiconductor layer to a second surface of said first semiconductor layer contacting said second semiconductor layer, having a width with respect to said surface of said second semiconductor layer, and extending along said surface of said second semiconductor layer for sectioning said second semiconductor layer into a plurality of blocks for isolation;

a wire with first and second ends on said surface of said second semiconductor layer, insulated from said second semiconductor layer except said first end which is connected to said surface of said second semiconductor layer at the inside of said surface, said second end extending to an edge of said semiconductor

substrate, said wire being useable for electrochemical etching said first semiconductor layer to form said hollow portion and said thin portion, wherein said wire does not cross said impurity diffusion layer except at said second end.

2. The semiconductor device as claimed in claim 1, wherein said impurity diffusion layer has a C-shape portion in respect of said surface of said second semiconductor substantially surrounding said thin portion, said wire extends to the inside of said C-shaped portion through an opening of said C-shaped portion, and said first end is connected to said second semiconductor layer at said inside of said C-shaped portion.

3. The semiconductor device as claimed in claim 2, wherein said impurity diffusion layer further extends from both ends of said C-shaped portion to a peripheral of said semiconductor substrate in parallel as first and second portions, respectively, and further extend along edges of said semiconductor substrate to have an outer C-shape around said C-shape portion, said wire extends from said first end at a space between said first and second portions.

4. The semiconductor device as claimed in claim 1, further comprising a diode in said second semiconductor layer, wherein said wire is connected to said second semiconductor layer through said diode to prevent a current from flowing from said second semiconductor layer to said wire.

5. The semiconductor device as claimed in claim 1, further comprising an insulation layer on said surface of said second semiconductor layer having a thickness t, said wire being arranged on said insulation layer to be insulated from said second semiconductor layer, a minimum distance between said wire and said impurity diffusion layer is larger than t except the edges of said semiconductor substrate.

6. A method of producing a semiconductor device comprising the steps of:

preparing a semiconductor wafer including a first semiconductor layer having a first conductivity and a second semiconductor layer having a second conductivity on said first semiconductor layer;

forming, at each chip unit, an impurity diffusion layer with said first conductivity piercing said second semiconductor layer from an surface of said second semiconductor layer opposite to said first semiconductor layer to a surface of said first semiconductor layer contacting said second semiconductor layer, having a predetermined width with respect to said surface of said second semiconductor layer, and extending along said surface of said second semiconductor layer for sectioning said second semiconductor layer into a plurality of blocks for insulation;

forming an integrated circuit portion on said surface of said second semiconductor layer at each chip unit;

forming, at each chip unit, a wire, at a first end, being connected to said second semiconductor layer at the inside of said chip unit and extending, at the second opposite end, to one of scribe lines defining said chip unit, wherein said wire between said first end and said second end of said wire does not cross said impurity diffusion layer except at said second end;

effecting electrochemical etching said first semiconductor layer with said wire to form said hollow portion and said thin portion; and

cutting said semiconductor wafer along said scribe lines.

7. A semiconductor device comprising:

a semiconductor substrate including a first semiconductor layer having a first conductivity and a second semiconductor layer having a second conductivity on said first semiconductor layer, said first semiconductor layer partially having a hollow portion in a first surface opposite to said second semiconductor layer, a surface of said second semiconductor layer opposite to said first semiconductor layer having first and second areas, said first area defined by a thin portion of said semiconductor substrate provided by said hollow portion, said second area being outside said first area;

an integrated circuit portion at said second area;

an impurity diffusion layer with said first conductivity piercing said second semiconductor layer from said surface of said second semiconductor layer to a second surface of said first semiconductor layer contacting said second semiconductor layer,

having a width with respect to said surface of said second semiconductor layer, and extending along said surface of said second semiconductor layer for sectioning said second semiconductor layer into a plurality of blocks for isolation;

a wire with first and second ends on said surface of said second semiconductor layer, insulated from said second semiconductor layer except said first end which is connected to said surface of said second semiconductor layer at the inside of said surface, said second end extending to an edge of said semiconductor substrate, said wire being useable for electrochemical etching said first semiconductor layer to form said hollow portion and said thin portion, wherein said impurity diffusion layer has a C-shape portion in respect of said surface of said second semiconductor substantially surrounding said thin portion, said wire extends to the inside of said C-shaped portion through an opening of said C-shaped portion, and said first end is connected to said second semiconductor layer at said inside of said C-shaped portion, wherein said impurity diffusion layer further extends from both ends of said C-shaped portion to a peripheral of said semiconductor substrate in parallel as first and second portions, respectively and further extend along edges of said semiconductor substrate to have an outer C-shape around said C-shape portion, said wire extends from said first end at a space between said first and second portions, and wherein said wire does not cross said impurity diffusion layer except at a non-edge portion of said surface of second semiconductor layer.